NR

Code No: A5704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, October / November-2011

ELECTRONIC DESIGN AUTOMATION TOOLS

(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) List out different data types available in Verilog for connectivity and storage, by giving heir syntax. [6]

b) Write Verilog code for 4-bit ripple carry adder. [6]

2.a) Distinguish between procedural, procedural-continuous, and non-blocking assignments. [6]

b) Write Verilog code for 3-bit up-down counter. [6]

3.a) Write the differences between function calls and task calls with suitable examples. [6]

b) Write a Verilog code to count number of 1's in a given binary word. [6]

4.a) With the help of neat flow diagram explain various simulations available in Verilog. [6]

b) Write a synthesizable Verilog code for 2-bit comparator. [6]

5. Describe the modeling of Moore and Mealy finite state machines with suitable examples. [12]

6.a) Explain about the following p-spice commands with syntax and examples:
1) .DC 2) .PLOT 3).OP [6]

b) Draw the op-amp integrator circuit and write the spice code taking op-amp dc model. [6]

7. Describe the mixed signal simulation process for D-to-A Converter by explaining various steps involved. [12]

8.a) Discuss about various issues involved in high speed PCB design. [6]

b) Write about ORCAD Deign entry tool. [6]

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